AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

doping a first region of a semiconductor substrate;

incising the substrate to provide an array of edges having substantially vertical edge surfaces, pairs of the edge surfaces facing one another and spaced apart a distance equal to one half of a pitch of the array of edges;

doping second regions between the pairs of edge surfaces;

disposing respective structures each providing an electronic memory function on at least some respective ones of the edge surfaces, the structure is composed of an oxide-nitride-oxide structure formed under a control gate such that the nitride is adapted to be a charge storage layer; and

establishing electrical contacts to the first and second regions.

2. (Original) The method of claim 1, wherein disposing comprises:

forming ONO structures on at least some respective ones of the edge surfaces; and

creating respective gates on the ONO structures.

3. (Original) The method of claim 1, wherein disposing comprises:

forming ONO structures on at least some respective ones of the edge surfaces; and

creating respective gates on the ONO structures, wherein forming ONO structures comprises:

growing silicon dioxide from silicon comprising the edge surfaces;

forming a silicon nitride layer on the silicon dioxide; and

forming silicon dioxide on the silicon nitride.

4. (Original) The method of claim 1, wherein disposing comprises forming respective polysilicon gates on respective ones of the surface edges.

5. (Original) The method of claim 1, wherein disposing comprises:

forming a first gate dielectric on the surface edge;

forming a floating gate on the first gate dielectric;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

6. (Original) The method of claim 1, wherein disposing comprises disposing structures comprising gates each configured to store more than one bit per gate.

7. (Original) The method of claim 1, wherein disposing comprises:

forming a first gate dielectric on the surface edge;

forming a floating gate on the first gate dielectric, wherein the floating gate is configured to store more than one bit per floating gate;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

8. (Original) The method of claim 1, wherein disposing comprises:

forming ONO structures on at least some of the edge surfaces; and

creating respective gates on the ONO structures, wherein the structures providing the electronic memory function are configured to store more than one bit per gate.

9. (Original) The method of claim 1, wherein the semiconductor substrate comprises silicon.

10. (Original) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

disposing non-horizontal structures providing an electronic memory function spaced apart a distance equal to one half of a minimum pitch of the array; and

establishing electrical contacts to memory cells including the non-horizontal structures.

11. (Original) The method of claim 10, further comprising:

incising the substrate to provide an array of substantially vertical edge surfaces, pairs of the edge surfaces facing one another and spaced apart a distance equal to one half of a minimum pitch of the array of edges; and

doping second regions between the pairs of edge surfaces, wherein:

disposing comprises disposing the non-horizontal structures on the substantially vertical edge surfaces; and

establishing electrical contacts includes establishing electrical contacts to the first and second regions and to the non-horizontal structures.

12. (Original) The method of claim 11, wherein disposing the non-horizontal structures on the substantially vertical edge surfaces comprises:

forming ONO structures on at least some of the edge surfaces; and

creating respective gates on the ONO structures, wherein the structures providing the electronic memory function are configured to store more than one bit per gate.

13. (Original) The method of claim 11, wherein disposing the non-horizontal structures on the substantially vertical edge surfaces comprises:

forming ONO structures on at least some of the edge surfaces; and

creating respective gates on the ONO structures.

14. (Original) The method of claim 10, wherein the structures providing the electronic memory function are configured to store more than one bit per gate.

15. (Original) The method of claim 11, wherein disposing non-horizontal structures comprises:

forming a first gate dielectric on the edge surfaces;

forming a floating gate on the first gate dielectric, wherein the floating gate is configured to store more than one bit per floating gate;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

16. (Original) The method of claim 11, wherein disposing the non-horizontal structures on the substantially vertical edge surfaces comprises:

forming a first gate dielectric on the surface edge;

forming a floating gate on the first gate dielectric;

forming a second gate dielectric on the floating gate; and

forming a control gate on the second gate dielectric.

17. (Original) The method of claim 11, wherein disposing comprises forming respective polysilicon gates on the edge surfaces.

18. (Original) The method of claim 10, wherein disposing comprises forming respective polysilicon gates.

19. (Original) The method of claim 10, wherein disposing comprises disposing a structure that is configured to provide an electronic memory function by storing holes.

20. (Original) The method of claim 10, wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

21. (currently amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

disposing non-horizontal structures providing an electronic memory function spaced apart a distance equal to one half of a minimum pitch of the array, wherein the structures providing the electronic memory function are configured to store more than one bit per gate and are composed of an oxide-nitride-oxide gate dielectric formed under a control gate such that the nitride is adapted to be a charge storage layer; and

establishing electrical contacts to memory cells including the non-horizontal structures.

22. (Original) The method of claim 21, wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

23. – 112. (Canceled)